RECEIVED
CENTRAL FAX CENTER
JUN 09 2006

Patent

Customer No.: 31561
Docket No. : 9068-US-PA
Application No.: 10/064,095

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Applicant	: Chih-Wei Hung
Application No.	: 10/064,095
Filed	: June 11, 2002
For	: CMOS IMAGE SENSOR DEVICE AND PROCESS OF PRODUCING THE SAME
Art Unit	: 2811
Examiner	: MUNSON, GENE M.

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF UNDER 37 C.F.R. §41.37

+1-571-273-8300
(Via fax: 2+13 pages)

U.S. Patent and Trademark Office
Commissioner for Patents
Customer Window, Mail Stop **Appeal-Brief**
Randolph Building, 401 Dulany Street
Alexandria, VA 22314

Dear Sir,

In response to the Notification of Non-Compliant Appeal Brief dated May 12, 2006, Applicant hereby respectfully submits an amended Appeal Brief with corrections as required by the Examiner in said Notification.

Applicants are aware of the provisions set forth in 37 CFR 41.37(c)(1)(ii), reciting a statement identifying all other prior and pending appeals, interferences or judicial proceedings known to the related parties shall be made in an Appeal Brief. However, as indicated in the section "RELATED APPEALS AND INTERFERENCES" on page 2 of the Appeal Brief submitted by the Applicants, neither any related appeals nor interferences in connection with the above-identified application were submitted by the Applicants. And there were no relevant decisions rendered by a court or the Board in judicial proceedings, either. Similarly, Applicants have never presented any evidence under 37 CFR 1.130, 1.131, and 1.132. Hence, the originally-filed Appeal Brief included neither of the above.

Per the Examiner's requirement, Applicants added an "Evidence appendix" and a "Related proceedings appendix" to the previously-filed Appeal Brief under the provisions of 37 CFR 41.37 to avoid dismissal of the appeal. Attached herewith please find the amended Appeal Brief in 13 pages.

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Patent

Customer No.: 31561
Docket No. : 9068-US-PA
Application No.: 10/064,095

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date: June 9, 2006 By: Belinda Lee
Belinda Lee
Registration No.: 46,863

Please send future correspondence to:
7F. -1, No. 100, Roosevelt Rd.,
Sec. 2, Taipei 100, Taiwan, R.O.C.
Tel: 886-2-2369 2800
Fax: 886-2-2369 7233 / 886-2-2369 7234
E-MAIL: BELINDA@JCIPGroup.com.tw; USA@JCIPGroup.com.tw

RECEIVED
CENTRAL FAX CENTER
JUN 09 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

EX PARTE Chih-Wei Hung

Application for Patent

Filed: June 11, 2002

Serial No. 10/064,095

FOR:

CMOS IMAGE SENSOR DEVICE AND PROCESS OF PRODUCING THE SAME

(as amended)

AMENDED APPEAL BRIEF

JIANQ CHYUN Intellectual Property
Attorneys for Applicant

TABLE OF CONTENTS

		Page No.
I.	Real party in interest	1
II.	Related appeals and interferences	1
III.	Status of the claims	1
IV.	Status of amendments	1
V.	Summary of claimed subject matter	1
VI.	Grounds of rejection to be reviewed on appeal	2
	Were claims 8-16 properly rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka (2002/0039692)?	2
VII.	Arguments	2
A.	The related law	2
B.	Grouping of the claims	4
C.	*Claims 8-16 were improperly rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka (2002/0039692).*	4
D.	Conclusion.	7
VIII.	Claims appendix	9
IX.	Evidence appendix	11
X.	Related proceedings appendix	11

I. Real party in interest

The real party in interest is Powerchip Semiconductor Corp., the assignee of record.

II. Related appeals and interferences

There are no related appeals and/or interferences.

III. Status of the claims

A total of 15 claims were presented during prosecution of this application. Claims 8-15 have been cancelled. The Applicant appeals the rejected claims 1-7 and 16.

IV. Status of amendments

There have been no amendments to the claims filed subsequent to the final Office Action dated October 11, 2005 of the RCE application.

V. Summary of claimed subject matter

The claimed subject matter of independent claim 1 involved in the appeal is directed to a CMOS image sensor device as shown in Figures 1, 2 and 3F. Figures 3A-3F are cross-section views of the CMOS image sensor device of Figure 2 along the cutting line I-I. The CMOS image sensor device comprises a substrate 300 and an isolation structure 302 is formed on the substrate 300 ([0024], Figure 3A). The CMOS image sensor device also includes a photodiode sensing region 206 as in Figure 2 (in Figure 3, the N well 306 in the substrate 300), wherein the photosensing region 306 is located under the isolation structure 302 in the substrate 300 ([0022], [0025]). Moreover, a reset transistor 218, 326 is located on the substrate (Figures 2 & 3D-3F, [0022], [0029]), wherein the reset transistor has a source region 316a connected to a part of the photodiode sensing region (the region of the N well 306 and the substrate 300 in Figures 3D-3F). The CMOS image sensor device of the present

invention further comprises a local interconnect 212 as shown in Figure 2, wherein one end of the local interconnect 212 (324 in Figures 3D to 3F) is located on the substrate between the photodiode sensing region 206 and the reset transistor 218 (326 in Figure 3D). The one end of the local interconnect (212, 324) extends to an upper portion of the isolation structure 302 to cover a periphery of the isolation structure 302 over the photosensing region (the region of the N well 306 and the substrate 300 in Figures 3D-3F and 206 in Figure 2) and electrically connects to the source region 342 (through the contact 224 in Figure 2) of the reset transistor 326 (Figures 3D to 3F). As clearly illustrated in Figures 3D to 3F, the one end of the local interconnect 324 covers the periphery part of the isolation structure 302 that is over the photosensing region 306. The second end of the local interconnect 212 is located on the active region of the substrate to be used as a gate 222 of the source follower transistor (Figure 2, [0022] and [0029]).

VI. Grounds of rejection to be reviewed on appeal

Were claims 1-7 and 16 properly rejected under 35 U.S.C. 103(a) as being unpatenable the evidence being He et al. (USP 6,649,950), Chen et al. (USP 6,392,263), and Rhodes (USP 6,740,915), all considered together?

VII. Arguments

A. The related law

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." MPEP § 2143, 8th ed., February 2003.

A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art." 35 U.S.C § 103(a); see *Graham v. John Deere Co.*, 383 U.S. 1, 14, 86 S. Ct. 684, 15 L.Ed.2d 545, 148 USPQ 459, 465 (1966).

"The inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed." Hartness International, Inc. Vs. Simplimatic Engineering Co., 819 F2d 1100, 1108, 2 USPQ 2D 1826 (Fed. Cir. 1987).

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

"Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000).

"Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blue print for piecing together the prior art to defeat patentability—the essence of hindsight". *In re Dembiczak*, 175 F.3d at 999.

"It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention using the Applicant's structure as a template and selecting elements from the references to fill the gaps". *In re Gorman*, 933 F. 2d 982, 987, 18 USPQ 2d 1885 (Fed. Cir. 1991).

"The problem confronted by the inventor must be considered in determining whether it would have been obvious to combine references in order to solve that problem". In re Diversitech Corp. Vs. Century Steps, Inc., 850 F. 2d 675, 679, 7 USPQ 2d 1315 (Fed. Cir. 1988).

Finally, if an independent claim is nonobvious under 35 U.S.C.§103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d, 1596 (Fed. Cir. 1988).

B. Grouping of the claims

For the only ground of rejection contested by appellant in this appeal, claims 1-7 may be treated as one group, and independent claim 1 may be taken as representatives for the issue on appeal.

C.

Claims 1-7 and 16 were improperly rejected under 35 U.S.C. §103(a) as being unpatenable the evidence being He et al. (USP 6,649,950), Chen et al. (USP 6,392,263), and Rhodes (USP 6,740,915), all considered together.

1. The rejection

Claims 1-7 and 16 have been rejected under 35 USC §103(a) as being unpatenable over He et al. (USP 6,649,950, He hereinafter), Chen et al. (USP 6,392,263, Chen hereinafter), and Rhodes (USP 6,740,915), all considered together. In making the rejection in the Office Actions dated June 21, 2004, November 29, 2004, May 3, 2005, and October 11, 2005, the Examiner basically contended that for an image device pixel as in Figure 1C of Chen, with the photodiode and reset transistor as in Figure 2 of He, it would have been obvious to use an "interconnect" 320 as in Rhodes, "extending to a upper portion of the isolation structure" 132, 332 as in Rhodes, in order to connect the n-type "source" region 210 of the reset transistor as in He to the gate of a source follower as in Rhodes and Chen. The Examiner also contended that the "photodiode sensing" region reads on a photodiode region 103 as in He. The "isolation structure" reads on a field oxide FOX as in He and field oxide

132 as in Rhodes. The Examiner further asserted on Page 3 of the Office Action dated October 11, 2005 that "local interconnect 212 does not cover the portion of "isolation structure 302" that is "over the photosensing region " 306, nor does claim 1 require such. In the same Office Action, the Examiner concluded that Rhodes (Figure 11) shows a "first end" at 315, an "isolation structure" and "a second end", while the present application shows no such section.

2. The prior art

The prior art reference Chen '263 relates to a highly integrated pixel comprising a photodiode formed by a n-well, with cathode, surrounded by a p-well; a reset transistor formed with its polysilicon gate positioned across p-well and n-well regions and it source merged with the photodiode cathode; and a sensing transistor with its source combined with drain of the reset transistor and its gate electrically connected to the source of the reset transistor. In brief, Chen's invention is directed to reducing the photodiode leakage current because no n+/p-well junction is connected to the photodiode. The prior art reference He '950 basically discloses a photodiode being substantially covered with an overlying structure in the hopes of protecting the photodiode from surface damage. As shown in Figures 1-6, the periphery of the N+ region 103 is exposed by the isolation region (LOCOS or STI). The prior art reference Rhodes '915 teaches a pixel cell 30 that includes an oxide or other insulating film 318 deposited on the substrate. A doped region 315 is formed in the substrate as a floating diffusion region and a doped region 352 is formed in the substrate in the area that will later become the photodiode 350 as shown in Figure 8. Rhodes further teaches that a doped polysilicon layer 320 is deposited to form a buried conductor between the floating diffusion region 315 and the gate of a source follower transistor and to serve as the transistor gate for the source follower transistor. In brief, the buried contact of Rhodes decreases leakage form the diffusion region into the substrate and allows the source follower transistor be placed closer to the floating diffusion region.

3. The prior art differentiated

What significantly distinguishes the structure of this invention from the prior art references is that the present invention teaches forming a local interconnect, wherein one end

of the local interconnect 212, 324 covers the periphery of the isolation structure 302 that is disposed over the photosensing region as shown in Figures 2, 3F. With the periphery of the isolation structure, formed over the photodiode, being covered by the local interconnect, lattice damage to the periphery of photodiode node during the subsequent processes, such as ion implantation, etching of the spacer or plasma etching, can be prevented. Further the occurrence of dark current is minimized and the formation of white pixels in arrays of the CMOS image sensor device can be prevented. The Examiner in the Office Action dated October 11, 2005 asserted that Figures 2 and 3F of the application does not teach "local interconnect" line 212 covering the portion of "isolation structure "302 that is "over the photosensing region" 306, nor does claim require such. Applicants agree that the present invention is not directed to teach "local interconnect" line 212 covering the portion of "isolation structure "302 that is "over the photosensing region" 306. Instead, Applicants respectfully submit it is clear from Figures 2 and 3F and claim 1 of the application that the local interconnect line 212 covers the periphery of the isolation structure that is over the photosensing region 306, and not the central portion of the "isolation structure" 302 that is over the photosensing region 306. As a result, the periphery of the photosensing region 306 is protected by both the isolation structure and the first end of the local interconnect line 212. Further, the first end and the second end of the interconnect line 212 are clearly illustrated and defined in Figure 2 and in [0022].

Although the electrical circuitry of the image device pixel of Chen is similar to that of the instant case, the layout of the image sensor is completely different. Chen at least fails to teach or suggest a local interconnect as described in claim 1 of the instant case. Similar to Chen, He also fails to disclose a local interconnect wherein a first end is located between the photodiode sensing region and the reset transistor and extends to cover a periphery of the isolation structure that is over the photosensing region and electrically connect to the source region of the reset transistor, and a second end is used as a gate of a source follower transistor. Instead, He teaches a formation of a transfer gate 108 to cover the photodiode 112 not already covered by the FOX region.

The Office further relies on Rhodes to teach the local interconnect of the instant application. Rhodes teaches a deposition of a doped polysilicon layer 320 over the pixel cell 2 to form a buried conductor between a floating diffusion region 315 and the gate for the source follower transistor. Additionally the doped polysilicon layer 320 serves as the

transistor gate for the source follower transistor. The Office argued that the doped polysilicon layer 320 of Rhodes also cover a part of the isolation structure 332; however, as clearly demonstrated in Figures 8-11 of Rhodes, the section of the isolation structure 332 that is covered by the doped polysilicon layer 320 is not disposed over the photodiode 352. As a matter of fact, no part of the isolation structure 332 is over the photodiode 352 as shown in Figure 11.

Moreover, as stated in re *Diversitech Corp. Vs. Century Steps, Inc.*, "[t]he problem confronted by the inventor must be considered in determining whether it would have been obvious to combine references in order to solve that problem". Both Rhodes and Chen are not directed to protecting the surface of the photodiode from damage, the motivation to combine Rhodes or Chen is thus lacking. Although He teaches a method to cover the photodiode with an overlying structure, He fails to teach a photodiode sensing region formed under the isolation structure and the periphery of the isolation structure that is over an edge of the photosensing region is covered by one end of an local interconnect.

4. Even if combined Chen, He, Rhodes

Since neither Chen, He nor Rhodes teaches or suggests at least a local interconnect, wherein a first end of the local interconnect extends to cover a periphery of the isolation structure that is over the photosensing region, Applicants respectfully submit that claim 1 defines over the prior art references for at least the reasons discussed above. If the independent claim 1 is allowable over the cited references, its independent claims 2-7 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1. In summary, Chen, He and Rhodes, neither alone nor in combination can possibly render the COMS image sensor device of the claimed invention obvious.

D. Conclusion

As noted, the Examiner has not properly applied 35 U.S.C. § 103 in his rejection of the claims at issue. Accordingly, Applicants believe that the rejections under 35 U.S.C. § 103 to be in error, and respectfully request the Board of Appeals and interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully submitted,

Date : June 9, 2006

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw

VIII. Claims appendix

CLAIMS ON APPEAL:

1. (previously presented) A complementary metal oxide semiconductor (CMOS) image sensor device comprising:

a substrate;

an isolation structure formed on the substrate;

a photodiode sensing region formed under the isolation structure in the substrate;

a reset transistor located on the substrate, wherein the reset transistor has a source region connected to a part of the photodiode sensing region; and

a local interconnect, wherein a first end of the local interconnect is located on the substrate between the photodiode sensing region and the reset transistor, extending to an upper portion of the isolation structure to cover a periphery of the isolation structure over the photosensing region and electrically connect to the source region of the reset transistor, and a second end of the local interconnect is located on the active region of the substrate to be used as a gate of a source follower transistor.

2. (original) The CMOS image sensor device of claim 1, wherein the photodiode sensing region is located under the isolation structure.

3. (previously presented) The CMOS image sensor device of claim 1, wherein a spacer is formed on a sidewall of the local interconnect.

4. (previously presented) The CMOS image sensor device of claim 1, wherein the photodiode sensing region further comprises a doped region with a conductivity type same as that of the source region of the reset transistor.

5. (previously presented) The CMOS image sensor device of claim 1, wherein a P type well is further formed under the reset transistor.

6. (previously presented)The CMOS image sensor device of claim 1, wherein the substrate is a first type conductivity substrate and the photodiode sensing region comprises a second type conductivity doped region.

7. (previously presented)The CMOS image sensor device of claim 1, wherein the substrate is a P type substrate, and the photodiode sensing region comprises a deep N type well.

Claims 8-15 (cancelled)

16 (previously presented) The CMOS image sensor device of claim 1, wherein the source region is an n-type doped region.

IX. Evidence appendix

There is no evidence submitted pursuant to §§ 1.130, 1.131, or 1.132 of this title or of any other evidence entered by the examiner and relied upon by appellant in the appeal, along with a statement setting forth where in the record that evidence was entered in the record by the examiner.

X. Related proceedings appendix

There are no decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief.